REMARKS

The Examiner rejected claims 22-24 under 35 U.S.C. 112, first paragraph, as failing to comply with the written description.

The Examiner rejected claims 11-13, 14 and 17-24 under 35 U.S.C. §102(e) as being unpatentable over Jang et al. (US Pat. 6,869,858).

The Examiner rejected claims 14, 16 and 20 under 35 U.S.C. 103(a) as being unpatentable over Jang et al. (US Pat. 6,869,858).

Applicants respectfully traverse the §112 (first paragraph), §102(e) and §103(a) rejections with the following arguments.

35 USC § 112

The Examiner rejected claims 22-24 under 35 U.S.C §112, (first paragraph) stating: "The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The original disclosure does not include teaching 'removing, using a non-planarization process...' (claim 22, step (d)). As shown in Applicants specification (fig. 4 and [0024], the step of removing a fill layer 150 is performed by a planarization process."

In response, Applicants note that paragraph [0024] and FIG. 4 do not describe the Applicants invention, but rather describe a problem discovered by Applicants that can occur when a planarization process is used this point in the process which Applicants invention solves. Paragraph [0024] states "FIG. 4 is a partial cross-sectional view of semiconductor substrate **100** after a planarization process and illustrates non-uniform planarization of fill layer **150**. In FIG. 4, a planarization process has been performed."

However, Applicants invention is illustrated in Applicants FIGs. 5A, 5B, 6 and 7. Applicants paragraph [0030] states: "FIGs. 5A and 5B are partial cross-sectional views of semiconductor substrate **100** illustrating preparation of the substrate according to a first embodiment of the present invention prior to planarization. In FIG. 5A a photoresist mask **165** is formed over fill layer **150** in second region **140**. Photomask **165** may be formed by any of several methods well known in the art. In FIG. 5B, a wet etch is performed, reducing the size of and increasing the distance between the tops of hats **155** of FIG. 5A to the size and spacing of hats **155A** of FIG. 5B." Applicants note that this supports "removing, using a non-planarization process, an uppermost layer of said fill material from over said first and second sets of trenches

and said top surface of said planarization stop layer, a thinned layer of said fill material remaining over said first and second sets of trenches and on said top surface of said planarization stop layer, said fill material still completely filling said first and second sets of trenches" of Applicants claim 20.

Applicants, therefore contend that the subject matter of claim 22 was clearly described in Applicants specification and request the 35 U.S.C. 112 (first paragraph) rejection of claims 22-24 be withdrawn.

35 USC § 102

The Examiner rejected claim 11 (and 13, 14 and 17-24) under 35 U.S.C §102(e) stating "Jang in figs. 6-11 disclose a method of fabricating a filled trench structure, comprising: forming a planarization stop layer 28 on a top surface of a substrate 10; forming a first set of trenches in a first region W2 of planarization stop layer and substrate and forming a second set of trenches in a second region W3 of planarization stop layer and substrate, trenches in first set of trenches having a higher aspect ratio than , trenches in second region (fig. 6 and col. 10, line 62 through col. 11, line 7); depositing a fill material 22 in first and second set of trenches and on a top surface of planarization stop layer 28, fill material completely filling trenches (col. 11, lines 8-28); removing an upper portion of fill material 22 by an etched back process (dry/wet etching) (fig. 7 and col. 11, lines 51-65); and (e) removing, using a planarization process, all fill material from top surface of planarization stop layer, a top surface of fill material in first and second sets of trenches co-planer with top surface of planarization stop layer (fig. 10)."

Applicants point out that Jang et al. describes two processes in FIGs. 6 through 11. The first process includes the steps illustrated in FIGs. 6, 7, 10 and 11 and the second includes the steps illustrated in FIGs. 6, 8, 9, 10 and 11, the difference being the substitution of the steps of FIGs. 9 and 10 for the step of FIG. 7.

First, Applicants contend that claim 11 is not anticipated by Jang et al. because Jang et al. does not teach each and every feature of claim 11. For example, Jang et al. does not teach "(d) after step (c), removing, using a non-planarization process, an uppermost layer of said fill material from over said first and second sets of trenches and said top surface of said planarization stop layer, a thinned layer of said fill material remaining over said first and second sets of trenches and on said top surface of said planarization stop layer, **said fill material still**

completely filling said first and second sets of trenches." Applicants respectfully point out that in FIG. 7 of Jang et al. fill layers 22a', 22b', 22c', and 22d' are not "completely filling the first and second trenches" as Applicants claim 11 requires. Applicants point out that top surfaces of fill layers 22a', 22b', 22c', and 22d' of Jang et al. FIG. 7 (and of FIG. 9 as well) are well below the top surface of the etch stop layers 28a, 28b, 28c and 28d (see Jang et al. FIG. 6). Further Jang et al. specifically teaches in col. 11, lines 55-59 referring to FIG. 7, "there has been etched back the blanket aperture fill layer 22 such that the thickness of the blanket aperture fill layer 22a', 22b', 22c', and 22d' within the apertures has been reduced to thickness less than the height of the mesa H." See Jang et al. FIG. 6 for "H" which includes the etch stop layer. The Examiner should also note that Applicants claim 11 defines the trenches to include that portion through the etch stop layer as well as the portion in the substrate, to wit: "(b) forming a first set of trenches in a first region of said planarization stop layer **and** said substrate and forming a second set of trenches in a second region of said planarization stop layer **and** said substrate."

Second, Applicants contend that in Jang et al. the structure shown in FIG. 10 cannot be made from the structures shown in FIGs. 7 or 9. The Examiner indicated that FIG. 10 of Jang et al. taught "removing, using a planarization process, all fill material from top surface of planarization stop layer, a top surface of fill material in first and second sets of trenches co-planer with top surface of planarization stop layer (fig. 10)." Applicant point out that to get from FIG. 7 (or from FIG. 9) to FIG. 10 would require fills 22a', 22b', 22c', and 22d' to increase in thickness during the CMP process, which is impossible. While it is possible in Jang et al. to get to FIG. 10 from FIG. 8 directly, by skipping FIG. 9, this is taught as a CMP process and skips the wet etching steps of Jang et al. (see in col. 12, lines 48-56 of Jang et al., to wit " shown in FIG. 10...otherwise equivalent to the semiconductor integrated circuit...shown in FIG. 8 or FIG.

9 but where blanket fill dielectric layer 22a', 22b', 23c' and 22d'...have been chemical mechanical polish (CMP) planarized") which skips the requirement of Applicants claim 11, to wit "(d) after step (c), removing, using a **wet-etching, a dry etching, a reactive etching or a plasma etching process**, an uppermost layer of said fill material from over said first and second sets of trenches and said top surface of said planarization stop layer, **a thinned layer of said fill material remaining over said first and second sets of trenches** and on said top surface of said planarization stop layer."

Based on the preceding arguments, Applicants respectfully maintain that claim 11 is not unpatentable over Jang et al. and is in condition for allowance. Since claims 13-21 depend from claim 11, Applicants respectfully maintain that claims 13-21 are likewise in condition for allowance.

Applicants maintain the arguments presented *supra* with respect to claim 11 are applicable to claim 22 and that claim 22 is in condition for allowance. Applicants point out that Applicants claim 22 includes the limitation "(d) after step (c), removing, **using a non-planarization process**, an uppermost layer of said fill material from over said first and second sets of trenches and said top surface of said planarization stop layer, **a thinned layer of said fill material remaining over said first and second sets of trenches** and on said top surface of said planarization stop layer, said fill material still completely filling said first and second sets of trenches." Since claims 23 and 24 depend from claim 22, Applicants respectfully maintain that claims 23 and 24 are likewise in condition for allowance.

As to claim 14, Applicants contend that claim 14 is not anticipated by Jang et al. because Jang et al does not teach each and every feature of claim 14. For example, Jang et al. does not teach "between steps (c) and (d) forming a mask layer on said fill material in said second region, wherein in step (d) fill material is only removed from said first region." Applicants respectfully point out Jang et al., in FIG. 8 is removing fill material from the second region (22d'') not the first region 22a, 22b, and 22c, the exact opposite of what Applicants are claiming. Compare Jang et al. FIG. 8 with Applicants FIG. 5A and 5B.

Based on the preceding arguments, Applicants respectfully maintain that claim X is not unpatentable over Jang et al. and is in condition for allowance.

As to claim 17, Applicants contend that claim 17 is not anticipated by Jang et al. because Jang et al does not teach each and every feature of claim 17. For example, Jang et al. does not teach "wherein said first region is a memory cell array region and said second region is a support circuit region of an integrated circuit." Applicants contend the Examiner has provided no evidence that Jang et al. teaches "wherein said first region is a memory cell array region and said second region is a support circuit region of an integrated circuit" as Applicants claim 17 requires.

Based on the preceding arguments, Applicants respectfully maintain that claim 17 is not unpatentable over Jang et al. and is in condition for allowance.

As to claim 19, Applicants contend that claim 19 is not anticipated by Jang et al. because Jang et al does not teach each and every feature of claim 19. For example, Jang et al. does not teach "wherein the volume of fill material removed in step (d) is experimentally pre-determined to be a volume that allows removal in step (e) of all of said fill material from said top surface of

said substrate in both said first and second regions in a predetermined amount of chemical-mechanical-polish or grind time." Applicants contend the Examiner has provided no evidence that Jang et al. teaches "wherein the volume of fill material removed in step (d) is experimentally pre-determined to be a volume that allows removal in step (e) of all of said fill material from said top surface of said substrate in both said first and second regions in a predetermined amount of chemical-mechanical-polish or grind time" as Applicants claim 19 requires.

Based on the preceding arguments, Applicants respectfully maintain that claim 19 is not unpatentable over Jang et al. and is in condition for allowance.

As to claim 20, Applicants contend that claim 20 is not anticipated by Jang et al. because Jang et al does not teach each and every feature of claim 20. For example, Jang et al. does not teach "wherein step (d) removes about 5 to 20% of the as deposited thickness of said fill material.." Applicants contend the Examiner has provided no evidence that Jang et al. teaches "wherein step (d) removes about 5 to 20% of the as deposited thickness of said fill material." as Applicants claim 20 requires.

Based on the preceding arguments, Applicants respectfully maintain that claim 20 is not unpatentable over Jang et al. and is in condition for allowance.

As to claim 21, Applicants contend that claim 21 is not anticipated by Jang et al. because Jang et al does not teach each and every feature of claim 21. For example, Jang et al. does not teach "wherein step (d) reduces the **difference** between a volume of said fill material over first region and a volume of said fill material over said second region.." Applicants contend the Examiner has provided no evidence that Jang et al. teaches "wherein step (d) reduces the

difference between a volume of said fill material over first region and a volume of said fill material over said second region." as Applicants claim 21 requires.

Based on the preceding arguments, Applicants respectfully maintain that claim 21 is not unpatentable over Jang et al. and is in condition for allowance.

35 USC § 103 Rejections

As to claim 15, 16 and 20, Applicants have argued *supra* in response to the Examiners § 102(e) rejection of claim 11 that claim 11 is allowable, since claims 15, 16 and 20 depends from claim 11, Applicants respectfully maintain that claims 15, 16 and 20 are not unpatentable over Jang et al. and are in condition for allowance.

The Examiner rejected claims 15, 16 and 20 under 35 U.S.C §103 (a) stating that "Jang fails to disclose the fill material is removed about 5 to 20% of the as deposited thickness (claims 15&20); and the aspect ratio of the first/second trenches (claim 16). It would have been obvious to one with ordinary skill in the art at the time of the invention to perform an etched back process step as taught by Jang. The amount of the fill material being etched and the aspect ratio of the first/second trenches does not define patentable over Jang since it is well known processing variable and the discovery of the optimum or workable range involves only routine skill in the art. The specific amount of the semiconductor being etched does not provide any critical or unexpected results to the method of manufacturing a semiconductor device. Rather, it is merely an obvious selection of the etching amount based on desired functional characteristics determinable by routine experimentation. In Aller, the court stated, "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." *In re Aller,* 220 F.2d 454, 456 105 USPQ 233,235 (CCPA 1995)."

Based on the preceding arguments, Applicants respectfully maintain that claims 15, 16, and 20 are not unpatentable over Jang et al. and are in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0458.

Respectfully submitted,
FOR: Economikos et al.

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